IN THE SPECIFICATION

Please amend the specification as follows:

Page 2, paragraph 3:

In the advantageous embodiment of the communication system ~~as claimed in claim 2~~, a tolerance with respect to transmission errors that can be selected as required can be achieved, and a reliable synchronization can therefore be achieved, even given poor channels. On the one hand, chip errors can be corrected upon receiving a disturbed synchronization pattern owing to a sufficient Hamming distance between each possible valid data sequence of the time slot coding and the synchronization pattern. On the other hand, the probability of receiving a synchronization pattern by mistake can be kept low.

Page 2, paragraph 4:

In the advantageous embodiment of the invention ~~as claimed in claim 3~~, a new synchronization is performed when a specific threshold value for differences between the received data stream and the synchronization pattern is undershot or just reached. If the threshold value is, for example, $C$, it is then possible for $C$ errors that have possibly occurred during transmission of the pattern to be corrected. The synchronization pattern differs by a specific number of places from each possible data sequence of the time slot coding, independently of the chip delay thereof, in order that during normal time-slot-coded data transmission no false synchronization should occur through the random imitation of the synchronization pattern because of transmission errors. This number of places is also denoted the Hamming distance. If the magnitude of this number is $D$, transmission errors must therefore occur within the synchronization pattern length ($D$-$C$) for the synchronization pattern to be imitated. In order to ensure recognition of the transmitted synchronization pattern relative to the correct chip clock, the synchronization pattern additionally differs from all the shifted versions of the synchronization pattern and of the synchronization pattern with arbitrarily adjoining



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time-slot-coded data by a specific Hamming distance E which need not, however, necessarily correspond to the Hamming distance D.

Page 3, paragraph 3:

In the advantageous embodiment of the invention ~~as claimed in claim 5~~, the comparison of the received chip sequence with the stored synchronization pattern is performed with the aid of an *N*-phase shift register whose *N* parallel outputs are compared in pairs with the stored synchronization pattern, for example with the aid of equivalence gates. The outlay for the synchronization detector can be kept low, in particular by virtue of the fact that the addition of the equivalence gate outputs with leading "0" (non-correspondences) takes place only modulo $C + 2$.

Page 3, paragraphs 5-6:

The synchronization detector ~~as claimed in claim 6~~ can be implemented with particular ease and cost-effectively.

~~Claim 7 relates to a time-slot-coded signal according to the invention, and claim 8 to a relevant transmission method.~~



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